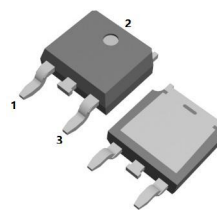
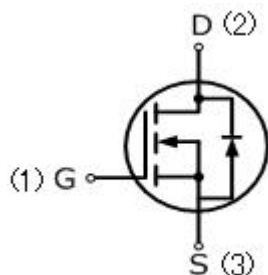


## 4N65(G,D)

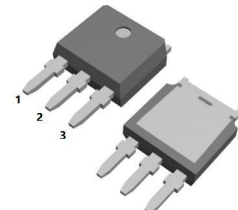
### 4 Amps,650 Volts N-CHANNEL Power MOSFET

#### FEATURE

- 4A,650V, $R_{DS(ON)MAX}=2.92\ \Omega$  @ $V_{GS}=10V/2A$
- Low gate charge
- Low  $C_{iss}$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-252-2L  
4N65G



TO-251-3L  
4N65D

#### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	4N65(G,D)	UNIT
Drain-Source Voltage	$V_{DSS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$I_D$	4	A
Pulsed Drain Current(Note1)	$I_{DM}$	16	
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	138	mJ
Reverse Diode dV/dt (Note 3)	dv/dt	5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55to+150	$^\circ\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

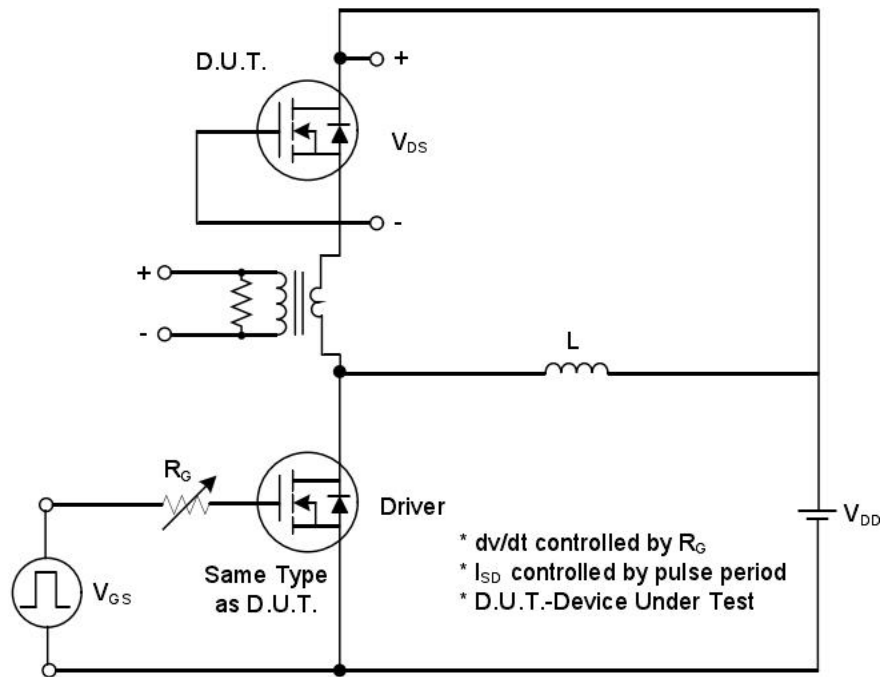
Parameter	Symbol	4N65(G,D)	Units
Thermal resistance , Channel to Case	$R_{th(ch-c)}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Power Dissipation	$T_C=25^\circ\text{C}$ $P_D$	75	W

Electrical Characteristics ( $T_c=25^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	650	—	—	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=650V, V_{GS}=0V$	—	—	1	$\mu A$
Gate-Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS}=30V, V_{DS}=0V$	—	—	100	nA
Gate-Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS}=-30V, V_{DS}=0V$	—	—	-100	nA
<b>On Characteristics</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	—	4.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$	—	2.431	2.92	$\Omega$
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	—	584	—	pF
Output Capacitance	$C_{oss}$		—	37	—	pF
Reverse Transfer Capacitance	$C_{rss}$		—	27	—	pF
<b>Switching Characteristics</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=325V, I_D=4A,$ $R_G=10\Omega$	—	10.4	—	ns
Turn-On Rise Time	$t_r$		—	1.2	—	ns
Turn-Off Delay Time	$t_{d(off)}$		—	21.6	—	ns
Turn-Off Fall Time	$t_f$		—	4	—	ns
Total Gate Charge	$Q_g$	$V_{DS}=520V, I_D=4A,$ $V_{GS}=10V$	—	12.8	—	nC
Gate-Source Charge	$Q_{gs}$		—	5.6	—	nC
Gate-Drain Charge	$Q_{gd}$		—	2.6	—	nC
<b>Drain-Source Body Diode Characteristics and Maximum Ratings</b>						
Continuous Diode Forward Current	$I_S$		—	—	4	A
Pulsed Diode Forward Current	$I_{SM}$		—	—	16	A
Diode Forward Voltage	$V_{SD}$	$I_S=2A, V_{GS}=0V$	—	—	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_{DS}=30V, I_F=1A,$ $dI_F/dt=100A/\mu s, (\text{Note3})$	—	125	—	ns
Reverse Recovery Charge	$Q_{rr}$		—	262	—	nC

#### Notes

1. Repetitive Rating: pulse width limited by maximum junction temperature.
2.  $V_{DD}=50V, L=10\text{mH}, R_g=25\Omega$ , starting  $T_j=25^\circ\text{C}$ .
3. Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

## RATING AND CHARACTERISTIC CURVES



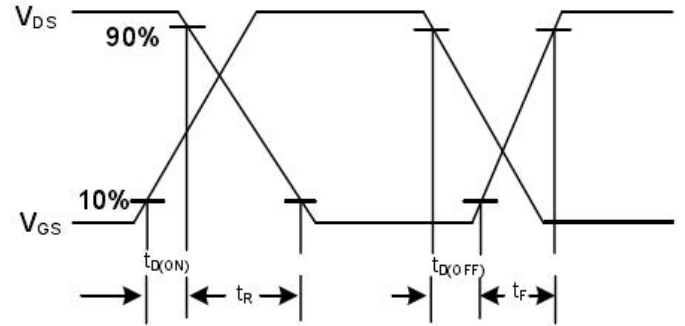
Peak Diode Recovery  $dv/dt$  Test Circuit



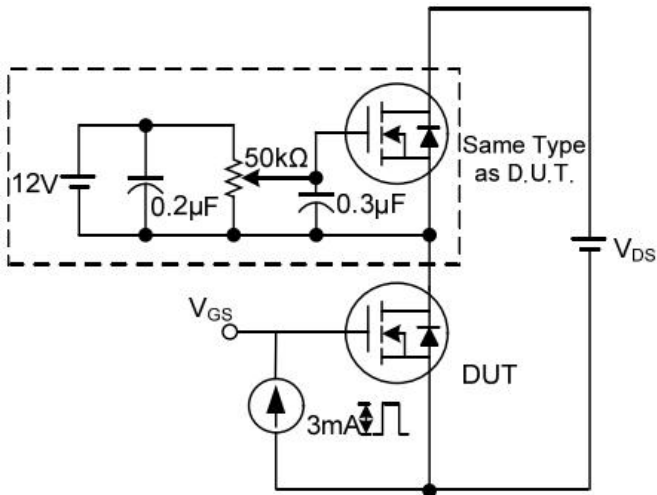
Peak Diode Recovery  $dv/dt$  Waveforms



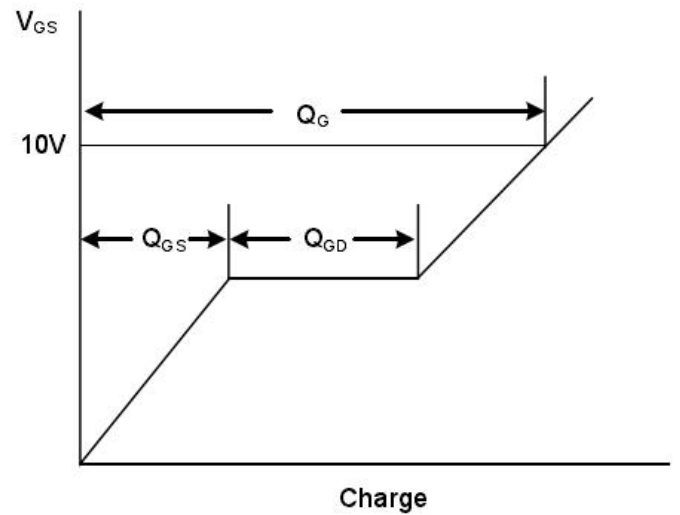
**Switching Test Circuit**



**Switching Waveforms**



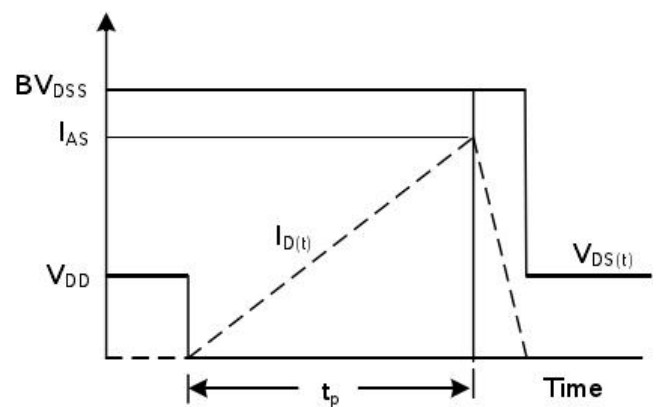
**Gate Charge Test Circuit**



**Gate Charge Waveform**



**Unclamped Inductive Switching Test Circuit**



**Unclamped Inductive Switching Waveforms**

## RATING AND CHARACTERISTIC CURVES

Figure.1 Typical Output Characteristics

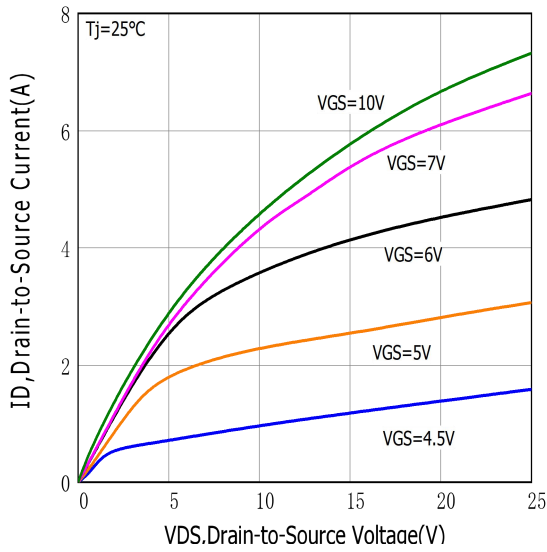


Figure.2 Typical Gate Charge vs Gate to Source Voltage

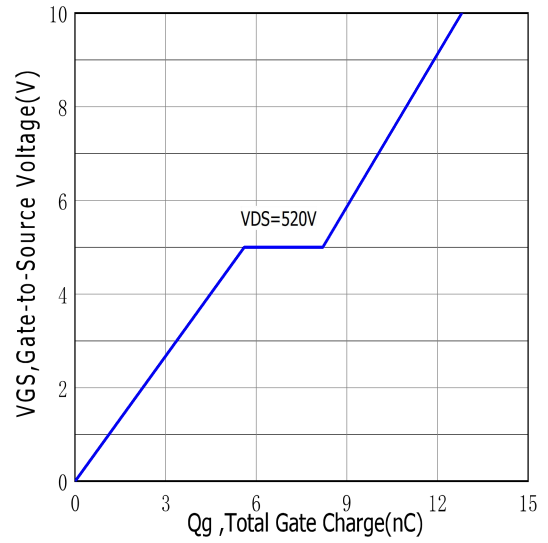


Figure.3 Typical Body Diode Transfer Characteristics

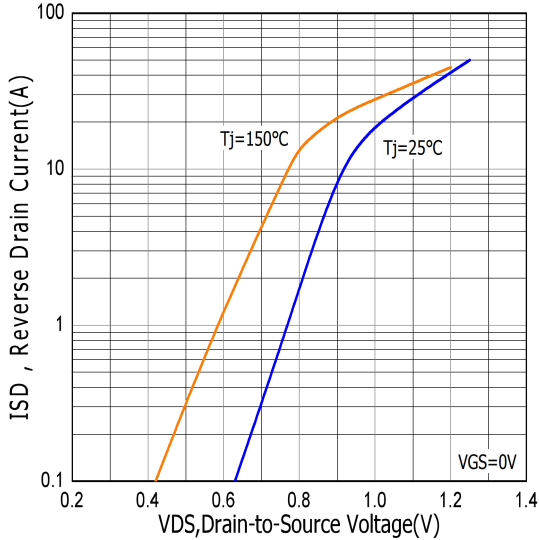


Figure.4 Typical Capacitance vs Drain to Source Voltage

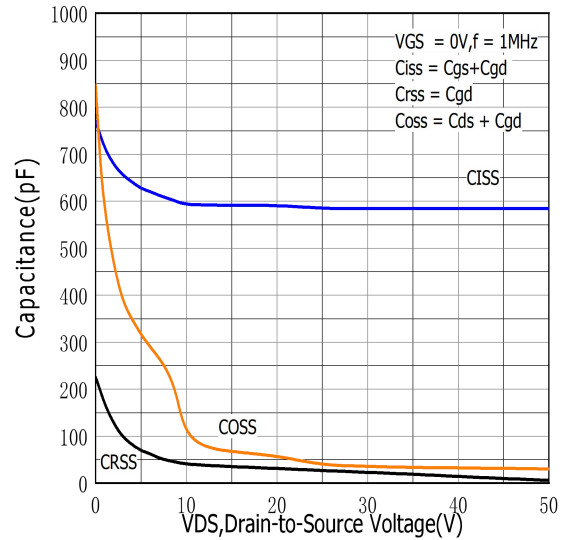


Figure.5 Typical Breakdown Voltage vs Junction Temperature

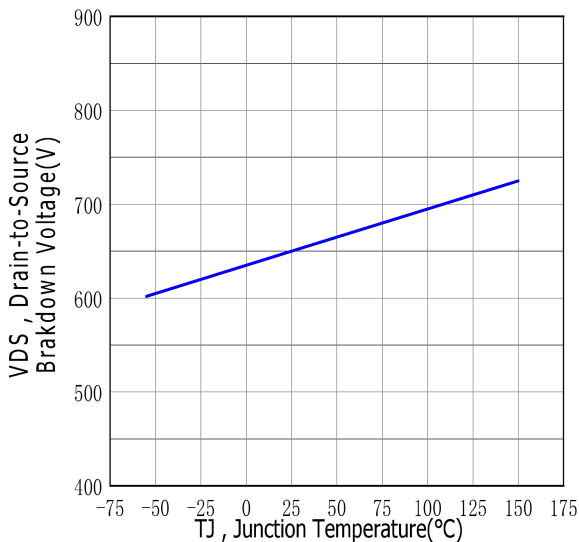


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

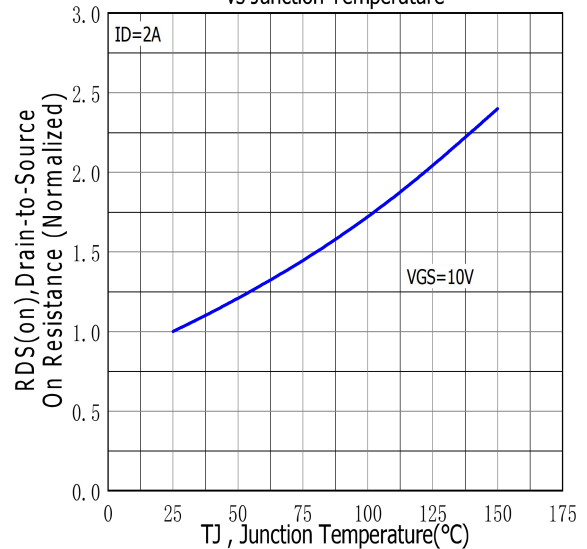


Figure.7 Maximum Forward Bias Safe Operating Area

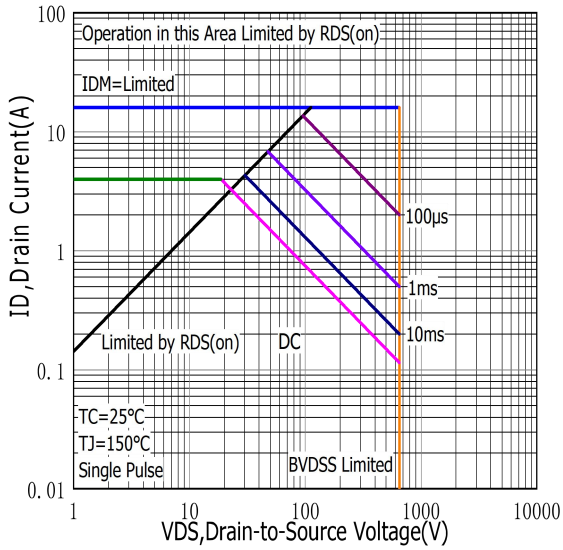


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

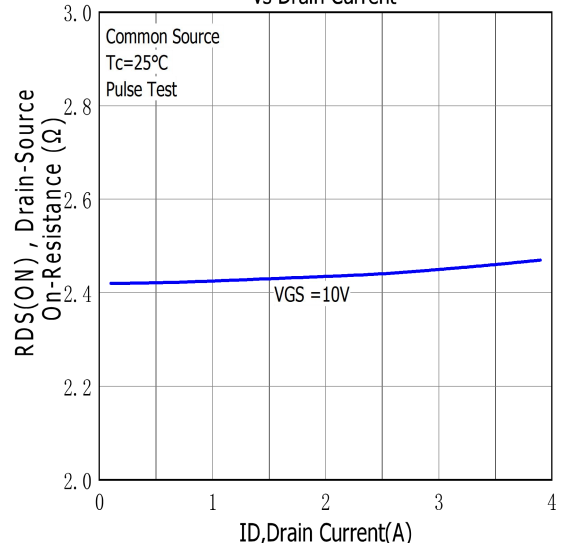


Figure.9 Maximum EAS vs Channel Temperature

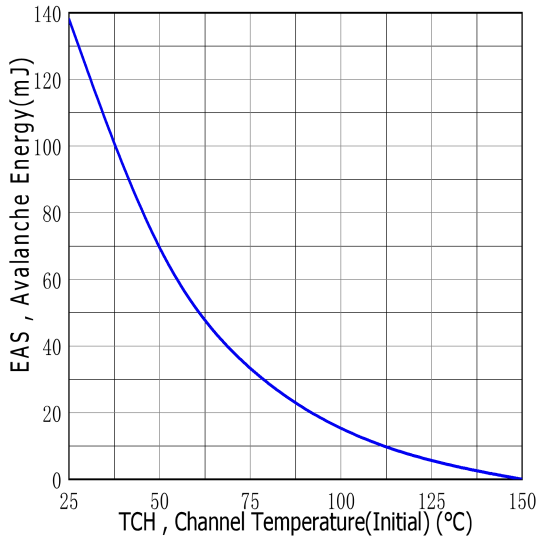


Figure.10 Typical Threshold Voltage vs Case Temperature

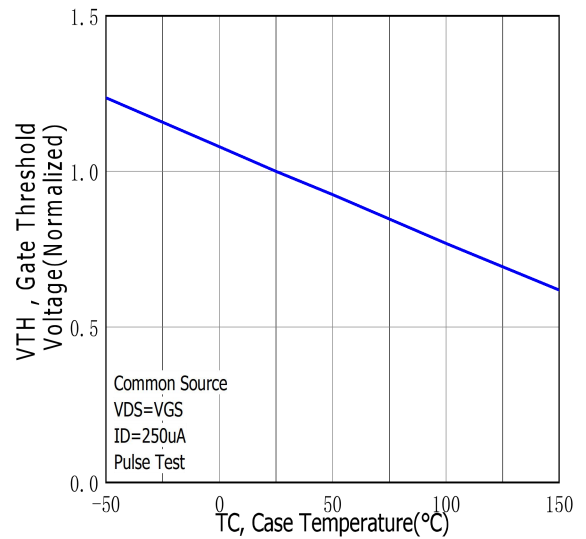


Figure.11 Maximum Effective Thermal Impedance, Junction to Case

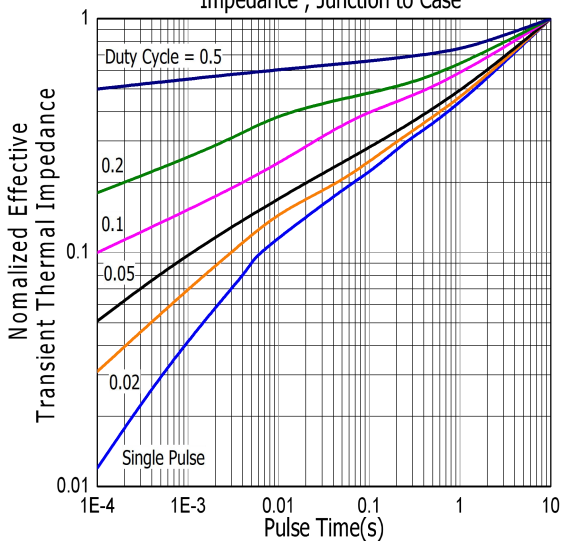
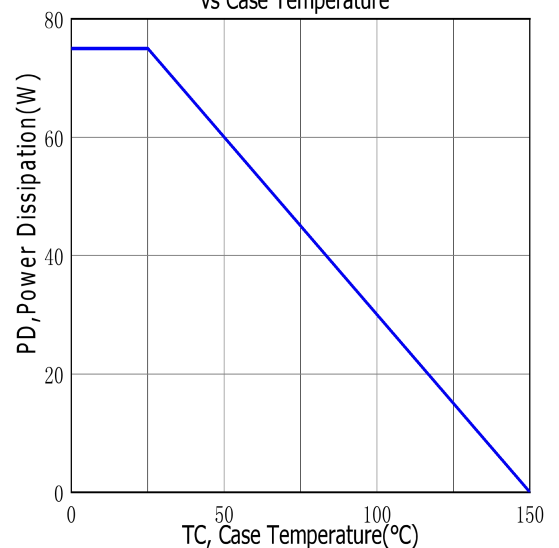
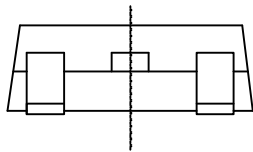
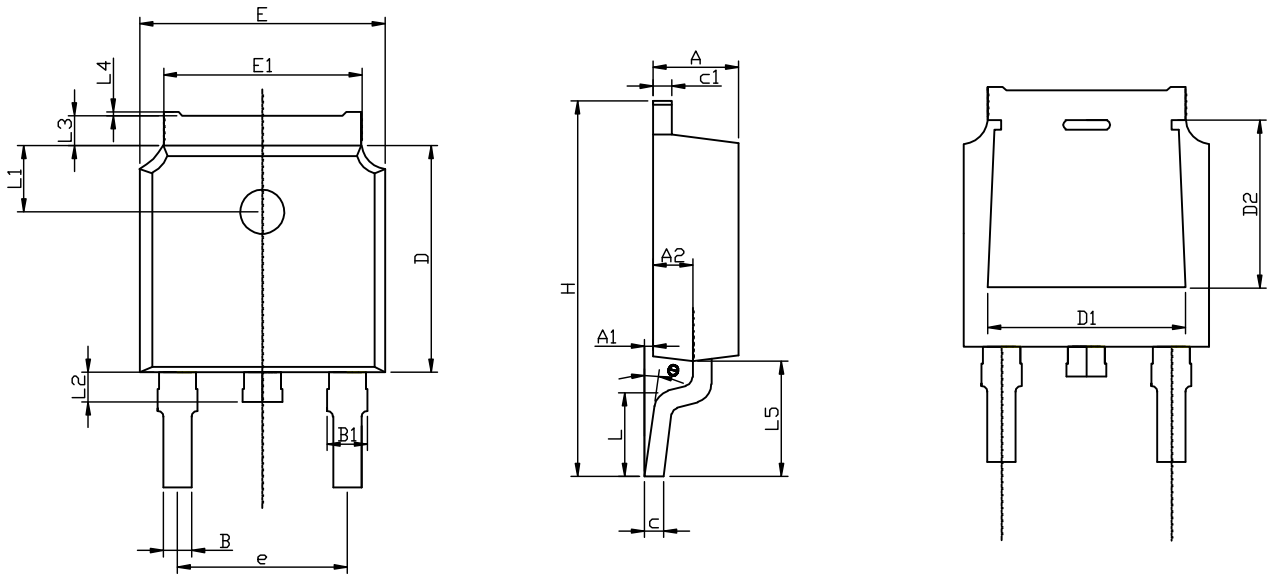


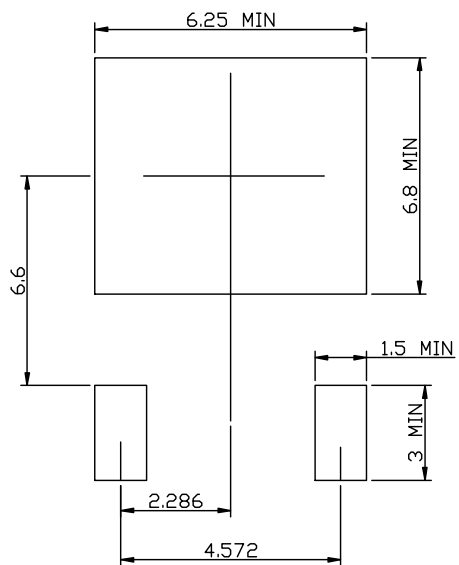
Figure.12 Maximum Power Dissipation vs Case Temperature



# TO-252-2L PACKAGE OUTLINE



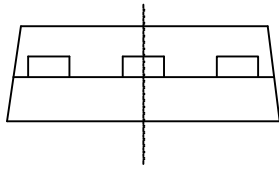
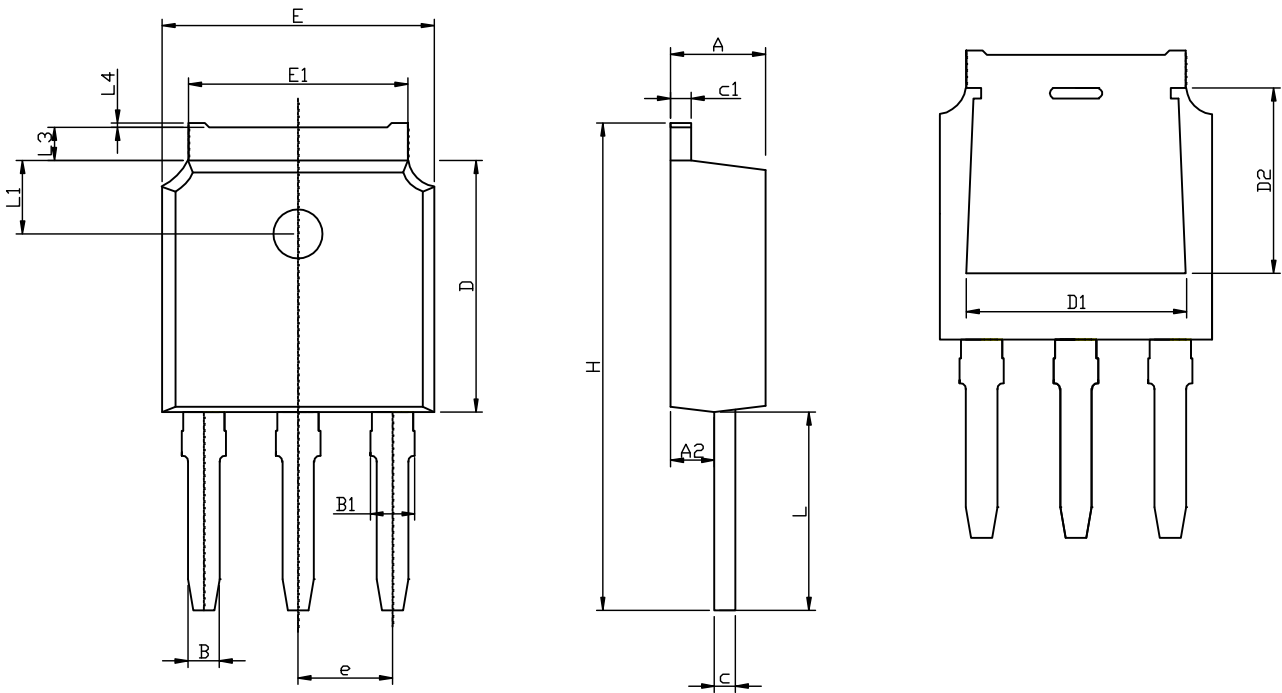
## RECOMMENDED LAND PATTERN



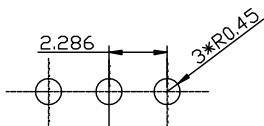
	MIN	NOM	MAX
A	2.15	2.30	2.45
A1	0.05	0.10	0.20
A2	0.91	1.07	1.22
B	0.66	0.76	0.86
B1	0.93	1.08	1.23
C	0.40	0.50	0.60
C1	0.40	0.50	0.60
D	5.95	6.10	6.25
D1	-	4.8REF	-
D2	-	3.8REF	-
E	6.45	6.60	6.75
E1	5.12	5.32	5.52
L		1.65	
L1	1.58	1.78	1.98
L2	0.60	0.80	1.00
L3	0.70	0.85	1.00
L4	0.00	0.05	0.20
L5	2.80	3.10	3.40
H	9.80	10.10	10.40
Θ	0°		8°
e		4.572REF	

UNIT: mm

## TO-251-3L PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

	MIN	NOM	MAX
A	2.15	2.30	2.45
A2	0.91	1.07	1.22
B	0.66	0.76	0.86
B1	0.93	1.08	1.23
C	0.40	0.50	0.60
C1	0.40	0.50	0.60
D	5.95	6.10	6.25
D1	-	4.8REF	-
D2	-	3.8REF	-
E	6.45	6.60	6.75
E1	5.12	5.32	5.52
L	4.50	4.80	5.10
L1	1.58	1.78	1.98
L3	0.70	0.85	1.00
L4	0.00	0.05	0.20
H	11.50	11.80	12.10
e		2.286REF	